UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,057	06/02/2001	Kambiz Hayat-Dawoodi	TI-29619	4012

7590 06/30/2004

Gary C. Honeycutt
Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265

EXAMINER	
KOBERT, RUSSELL MARC	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,057	HAYAT-DAWOODI, KAMBIZ	
	Examiner	Art Unit	
	Russell M Kobert	2829	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *6 and 10-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's arguments with respect to claims 1-5 and 7-9 have been considered but are moot in view of the new ground(s) of rejection and the finality of the rejection of the last Office is hereby withdrawn.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3-5 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Terada et al (5874773), website articles "Dominique François Jean Arago," "Arago's Disk" and R.A. Serway et al, "College Physics."

Terada et al anticipates a metallic leadframe structure (Figures 1 and 2) for use with a semiconductor chip (11a, 11b or 11c shown in Figures 3-5 respectfully) intended for operation in a changing magnetic field, comprising: a chip mount pad (2; col 4, ln 41-43) having at least one slit (9; col 5, ln 1-2) penetrating the whole thickness of said pad (shown in Figure 7) and *substantially* traversing the area of said pad from one edge to the opposite edge (col 5, ln 7-10; "the tips 9a of the slit 9 shape extend toward the outer periphery of the die pad 2" thus *substantially* traversing the area of the pad); and said slit wide enough to interrupt electron flow in the pad plane (considered an inherent effect of a slot located within a conductive material), but not wide enough to significantly reduce thermal conduction (col 7, ln 59 - col 8, ln 8) in a direction normal to said pad

plane, whereby said slit is operable to disrupt eddy currents (considered an inherent effect of a slot located within a conductive material) induced in said pad by said changing magnetic field; as recited in claim 1.

Terada et al anticipates a metallic leadframe structure (Figures 1 and 2) for use with a semiconductor chip (11a, 11b or 11c shown in Figures 3-5 respectfully) intended for operation in a changing magnetic field, comprising: a chip mount pad (2; col 4, ln 41-43) having a plurality of slits (9 and 10; col 5, ln 1-6) in a configuration operable to suppress eddy currents (considered an inherent effect of a slot located within a conductive material) induced in said pad by said changing magnetic field; each of said slits wide enough to interrupt electron flow in the pad plane (considered an inherent effect of a slot located within a conductive material), but not wide enough to significantly reduce thermal conduction (col 7, ln 59 - col 8, ln 8) in a direction normal to said pad plane; as recited in claim 8.

As to the inherency indicated supra, placing slots in a conductor such as a copper disk inherently interrupts the flow of induced eddy currents because the effect is a phenomenon of the laws of physics; discovered by Dominique François Jean Arago (1786-1853) in 1825. Of particular interest is the passage, which states "In this device, a copper disk is rotated rapidly with a hand crank and a step-up pulley system. Balanced on a pivot above the center of the disk is a compass needle. The motion of the needle relative to the highly conducting copper disk induces eddy currents in the disk. In turn, these eddy currents produce a torque on the magnetic needle, which starts to rotate. The presence of eddy currents may be inferred from the fact that a copper

disk with radial slots cut in it produces little effect; the slots interrupt the eddy currents." (Reference: "Dominique François Jean Arago, b. February 26, 1786, Estagel, Roussillon, France, d. October 2, 1853, Paris, France," page 3, First Paragraph, http://chem.ch.huji.ac.il/~eugeniik/history/arago.html and "Arago's Disk," http://physics.kenyon.edu/EarlyApparatus/Electricity/Aragos_Disk/Aragos_Disk.html). Moreover, the flow of electrons is a current, thus interrupting the flow of eddy currents further interrupts the flow of electrons. Further evidence of this naturally occurring phenomenon as a result of placing slots in a conductor such as a copper plate interrupts the flow of induced eddy currents, is disclosed in the college physics textbook "College Physics," by R.A. Serway et al. Such evidence can be found on pages 644-645, chapter 20.6, 3rd paragraph, that reads as follows: "If slots are cut in the metal plate, as in Figure 20.20, the eddy currents and the corresponding retarding force are greatly reduced. The cuts in the plate are open circuits for any large current loops that might otherwise be formed." See also MPEP 2131.01.

As to claim 3, having a structure comprising a sheet-like starting configuration having a thickness in the range from about 100 to 300 μm (col 4, ln 60-65) is anticipated.

As to claim 4, having a leadframe wherein said sheet-like starting configuration is selected from a group of metals consisting of copper, copper alloy, brass, aluminum, iron-nickel alloy, and invar (col 4, ln 45-46) is anticipated.

As to claim 5, having a pad with an area larger than the chip intended for mounting is anticipated (see Figures 3-5; note pad 2 has a larger area than chip 11a, 11b or 11c).

As to claim 9, having the plurality slits configured approximately parallel or approximately star-burst-like, or in any pattern suitable (col 5, ln 1-6; cross shape slit in combination with the plurality of radially arranged slits) for suppressing the origin of eddy currents, while preserving the mechanical stability and thermal conduction of said leadframe (in order to maintain an anticipated amount of thermal conduction required by Terada et al, the die pad of the leadframe of Terada et al must maintain a degree of mechanical stability as disclosed in column 7, line 59 - column 8, line 55) is anticipated.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terada et al (5874773), website articles "Dominique François Jean Arago," "Arago's Disk" and R.A. Serway et al, "College Physics." as applied to claim 1 above, and further in view of Robinson et al (4952999).

Although Terada et al fails to disclose a slit having a width from about 0.01 to 0.5 mm as described in claim 2, Robinson et al shows a slotted metallic die attach pad

(Figures 3 and 4) for use with a die (24) intended for operation in a changing magnetic field, comprising: a chip mount pad (22) having at least one slit (25) penetrating the whole thickness of said pad (col 4, ln 18-22) and *substantially* traversing the area of said pad from one edge to the opposite edge (col 4, ln 26-27; also note the degree to which slots in Figures 3 and 4 extend across the die attach pad); and said slit wide enough to interrupt electron flow in the pad plane (considered an inherent effect of a slot located within a conductive material), wherein said slit is operable to disrupt eddy currents (considered an inherent effect of a slot located within a conductive material) induced in said pad by said changing magnetic field as described in claim 1, and further shows each slit having a width from about 0.01 to 0.5mm (col 4, ln 39-42; note: 0.5 mil converts to 0.0127 millimetre (mm) and 20 mils converts to 0.508 millimetre (mm)) as described in claim 2.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the teachings of Robinson et al with that of Terada et al to make the claimed invention because each utilizes slots in a leadframe to compensate for differences in thermal stress between a chip and a chip mount pad and one having ordinary skill would have been motivated to combine these teachings because reducing undue stress results in improved electrical performance and reliability between a chip and leadframe structure.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terada et al (5874773), website articles "Dominique François Jean Arago," "Arago's Disk" and

R.A. Serway et al, "College Physics." as applied to claim 1 above, and further in view of Parker et al (6087842).

Although Terada et al fails to disclose the chip having an integrated circuit including a hall device, Parker et al discloses and integrated circuit on a leadframe having a hall device in the integrated circuit (see Abstract) as described in claim 7.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the teaching of Parker et al with that of Terada et al because integrating test probes such as Hall devices within an integrated circuit provides improved fault detection between integrated circuit bonding pads and a leadframe that yields greater reliability and measurement accuracy of interconnection faults and provides measurements of externally inaccessible regions.

7. A shortened statutory period for response to this action is set to expire three month(s) from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell Kobert whose telephone number is (571) 272-1963. The Examiner's Supervisor, Kammie Cuneo, can be reached at (571) 272-1957. For an automated menu of Tech Center 2800 phone numbers call (571) 272-2800.

Russell M. Kobert
Patent Examiner
Group Art Unit 2829
June 17, 2004

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800